Enabling 22-nm Logic Node with Advanced RET Solutions

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ABSTRACT

The 22-nm technology node presents a real breakthrough compared to previous nodes in the way that state of the art scanner will be limited to a numerical aperture of 1.35. Thus we cannot "simply" apply a shrink factor from the previous node, and tradeoffs have to be found between Design Rules, Process integration and RET solutions in order to maintain the 50% density gain imposed by the Moore's law. One of the most challenging parts to enable the node is the ability to pattern Back-End Holes and Metal layers with sufficient process window. It is clearly established that early process for these layers will be performed by double patterning technique coupled with advanced OPC solutions.

In this paper we propose a cross comparison between possible double patterning solutions: Pitch Splitting (PS) and Sidewall Image Transfer (SIT) and their implication on design rules and CD Uniformity. Advanced OPC solutions such as Model Based SRAF and Source Mask Optimization will also be investigated in order to ensure good process control.

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Keywords: Logic 22nm, Pitch Splitting, SIT, SMO, Model Based SRAF

1. INTRODUCTION

Back End Of Lines (BEOL) layers become the most critical layers for 32nm logic node and beyond. The introduction of regular design rules on Gate layers induce an increase of design complexity on contact and metal trenches patterning. In order to maintain the "natural density shrink" of the Moore's law, the ITRS roadmap indicates the necessity to print trenches period of 90nm for the 32nm logic technology nodes and 64nm pitches for the 22nm technology nodes[1]. It is a great challenge because EUV technology is still not fully ready for industry purpose, and will be used in a second phase. It is clearly established now that in a first phase the technology nodes, from 32nm to 22nm, will be manufactured without any improvement of the optical performance of the scanner. Thus, state of the art scanner will be limited to a numerical aperture of 1.35 and immersion at a wavelength of 193nm. Simply considering the Rayleigh criterion, which shows a theoretical resolution limit of 71nm (80nm in practice), it appears that 22nm logic nodes require to print sub resolved features. Double patterning scheme is mandatory to overcome this challenge. Double Dipole Lithography (DDL) can be dropped out because although it has proven good process window margin for Metal patterning, this method is applicable only on feature above the resolution limit[2]. Dark field mask and positive tone development resist are limiting factors for double patterning in a way that it is limited to print small trenches in a semi-dense configuration[3]. Such process is not capable to print below 60nm trenches and it is necessary to add chemical shrink[4] which is pain full for process cost. The only viable solutions for patterning sub-resolved trench layers are pitch splitting with tone inversion or self-aligned double patterning process. We propose in this paper to compare two decomposition types: Litho – Etch – Litho – Etch (LELE) process scheme with negative tone developer (NTD), and Sidewall Image Transfer (SIT) with spacer on resist process as described in Figure 1 in the case of MetalX (Mx) jog structure.

The first decomposition is a direct one, in the sense where you "only" have to split the pitch and what you see on both lithographic steps is what you get on wafer after the full process (Figure 1.a). The two others are indirect

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decompositions with the first lithographic step that permits to define structure supporting spacer deposition and second lithography extra features removal. One particularity of the SIT process is the possibility to pattern the 1st lithographic step on both ways as described in Figure1.b and Figure1.c and resulting in the same output. It is due to the fact that lines at half pitch are derived from the 1st lithographic lines at pitch after spacer deposition process. In that sense pitch's lines and half pitch lines can be reversed.

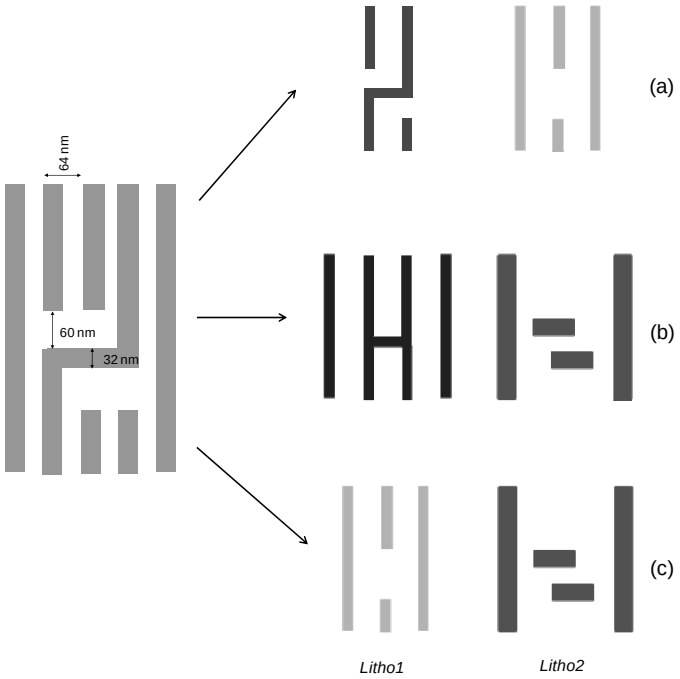


Figure 1 – Splitting comparison for Metal jog structure with 1st litho on the left and 2nd litho on the right; **a)** double patterning with LELE scheme, **b)** Sidewall Image Transfer 1st decomposition (SIT1), **c)** Sidewall Image Transfer 2nd decomposition (SIT2)

We propose to compare these two decomposition style (1 LELE and 2 SIT) on 64nm pitch Mx jog structure with 32nm line and 60nm of gap.

2. DOUBLE PATTERNING PROCESS FLOW

The number of steps increase in a double patterning flow regarding standard single patterning process. We can count 2 steps with one lithographic and one etch step in a single patterning flow. On the Figure 2 we have reported the process flow in the case of pitch splitting method with Litho-Etch-Litho-Etch process flow.

For this LELE we have five steps with two consecutive litho-etch steps and one alignment step between the first and second exposure. On this figure we have reported the case of the Mx jog. The first lithographic step (*Litho1*) consists in printing trenches within resist deposit on a hard mask. The first etch step (*Etch1*) permits to transfer the trench into the hard mask. Then this operation is repeated after alignment of the second mask and resist's film deposition, with trench patterning (*Litho2*) and transfer into hard mask (*Etch2*).

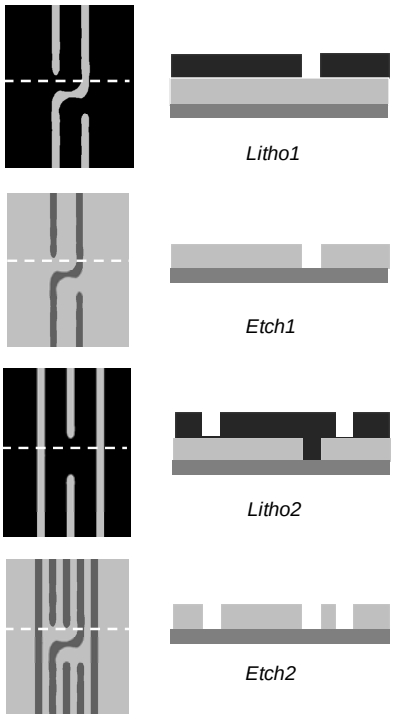


Figure 2 – Process flow for a double patterning scheme based on Litho-Etch-Litho-Etch (LELE) process

For the SIT we can list six consecutive steps. On the Figure 3 we have reported the four principal steps of the process flow for both decomposition (SIT1 and SIT2). The first lithographic step consists in patterning line of resist on top of a hard mask (*Litho1*). A spacer deposition is performed during the second step (*Spacer*) with a etch back and stripping process to remove supporting line of resist. Thus it remains spacer features at half pitch regarding line of resist of the 1st lithographic step. The spacer profile depends on the 1st lithographic step as highlighted between Figure 3.a and Figure 3.b. The second mask is then aligned and exposed in order to create plug of resist in the extra features area (*Litho2*). By this way we can define the metal line-end as well as removing dummies supporting line used for spacer growth. Then the final etch transfer the pattern within the hard mask defining the Mx jog structure requested (*Etch*).

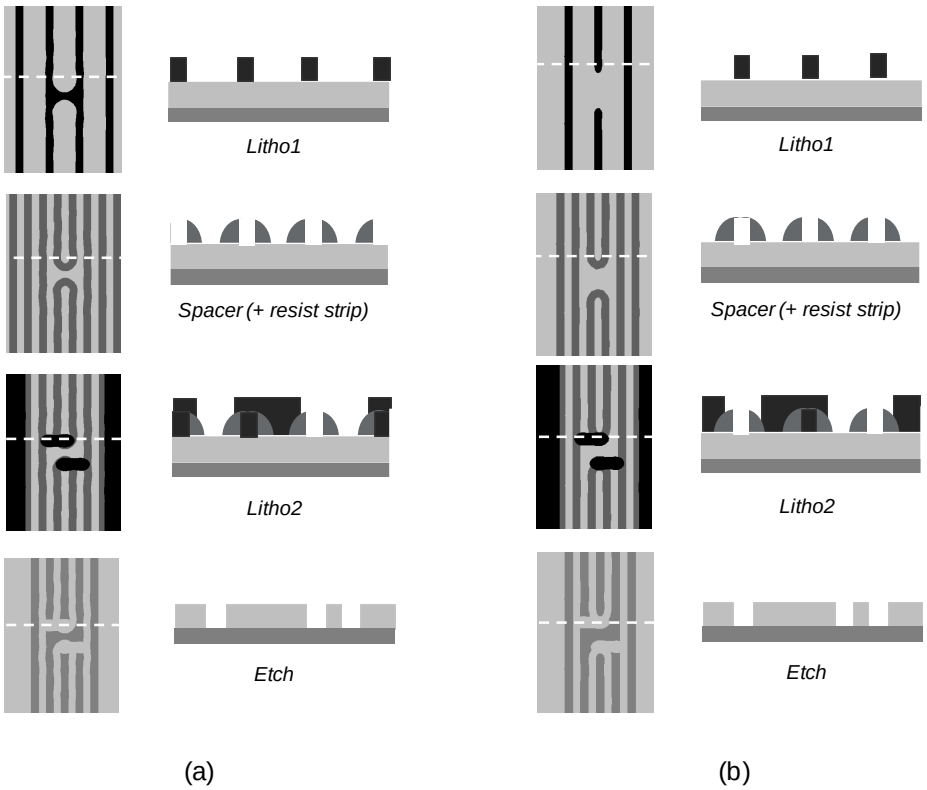


Figure 3 – Process flow for a double patterning scheme based on SIT process flow (Litho-Spacer-Litho-Etch); **a)** 1st SIT decomposition type (SIT1), **b)** 2nd SIT decomposition type (SIT2). Between these 2 decomposition only the Litho1 step is different

By looking at the final outputs between LELE, SIT1 and SIT2 we can see some obvious differences on the contour shapes. Actually LELE structures present rounded line-end whereas SIT has straight line-end definition due to the fact that it is cut by the second exposure. Moreover we can see some risk of pinching on horizontal line of the 2D shape for LELE and SIT1 whereas this risk is minimized on SIT2.

These contour differences highlight the fact that CD variability will be dependent on the double patterning scheme that will be used. Thus we propose to compare the CD uniformity for each of these decompositions.

3. CD UNIFORMITY CALCULATION

We propose to use an edge-based method to determine the CD uniformity apply on 2D jog structures. The principle is to take into account independently the CDU contribution from each edge considering the 3σ variability from lithography budget and process step (etch, overlay, etc…). The CDU calculation for a gap between line-ends of two consecutive lithographic steps is describe on the Figure 4.

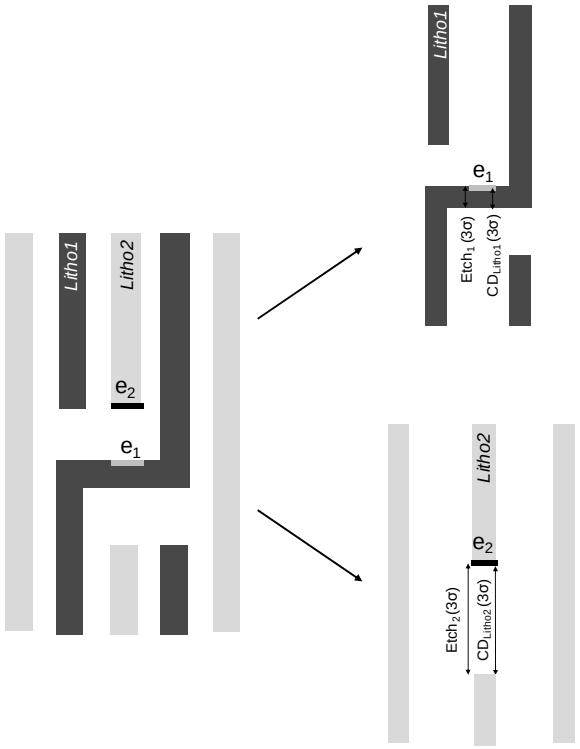


Figure 4 – Edge-based CD uniformity calculation method. CD variability (3σ) from each edge are independently taken into account and then recombined to determine the final CDU (3σ) between edges e_1 and e_2

On this figure, we consider that the CDU (3σ) of the gap between edges e_1 and e_2 (gap e_1-e_2) is impacted by the variability of edge e_1 from the *Litho1* step, including respectively half of CD_{Litho1} (3σ) and $Etch_1$ (3σ) from lithographic and etch dispersion, and the variability of edge e_2 from *Litho2* step (driven by half of CD_{Litho1} (3σ) and $Etch_1$ (3σ)). On top of that we have also to consider the variability coming from the overlay between *Litho1* and *Litho2*. Considering all these variability we can derive a global CD uniformity (3σ) between edges of two different exposure steps as mention in Equation (1).

$$Gap_{e_1-e_2}(3\sigma) = \sqrt{\left(\frac{CD_{Litho1}}{2}\right)^2 + \left(\frac{Etch_1}{2}\right)^2 + OVL^2 + \left(\frac{CD_{Litho2}}{2}\right)^2 + \left(\frac{Etch_2}{2}\right)^2} \quad (1)$$

Then we can apply this global CDU calculation to the three different kinds of splitting strategy: LELE, SIT1 and SIT2. We propose to look deeper on the variability of the gaps between line-ends and 2D shape (*Gap1* and *Gap2*) as well as horizontal line of the 2D shape (*Line*). On the Figure 5 we have reported these three decomposition style with the corresponding lithographic steps and the CD variability needed for the calculation.

For the LELE process scheme (Figure 5.a) we can calculate the CDU for *Gap1*, *Gap2* and *Line* as a function of the CD_1 and CD_2 of first lithographic step and CD_3 of second one. The equation (2) permits to determine the 3σ CD variability for the Gap1 where we can see that it is exclusively driven by the first patterning step. This variability is similar to a single patterning approach. The equation (3) represents the variability for the *Gap2* which is different from Gap1 in a sense where it is impacted by the double patterning steps. That's for why lithographic variation from each steps (CD_2 and CD_3) as well as etch of first and second patterning ($Etch_1$ and $Etch_2$) and overlay error (*OVL*) are taking into account. The Line variability is simply driven by the first patterning step with lithography (CD_2) and etching ($Etch_1$) contributions as detailed in Equation (4).

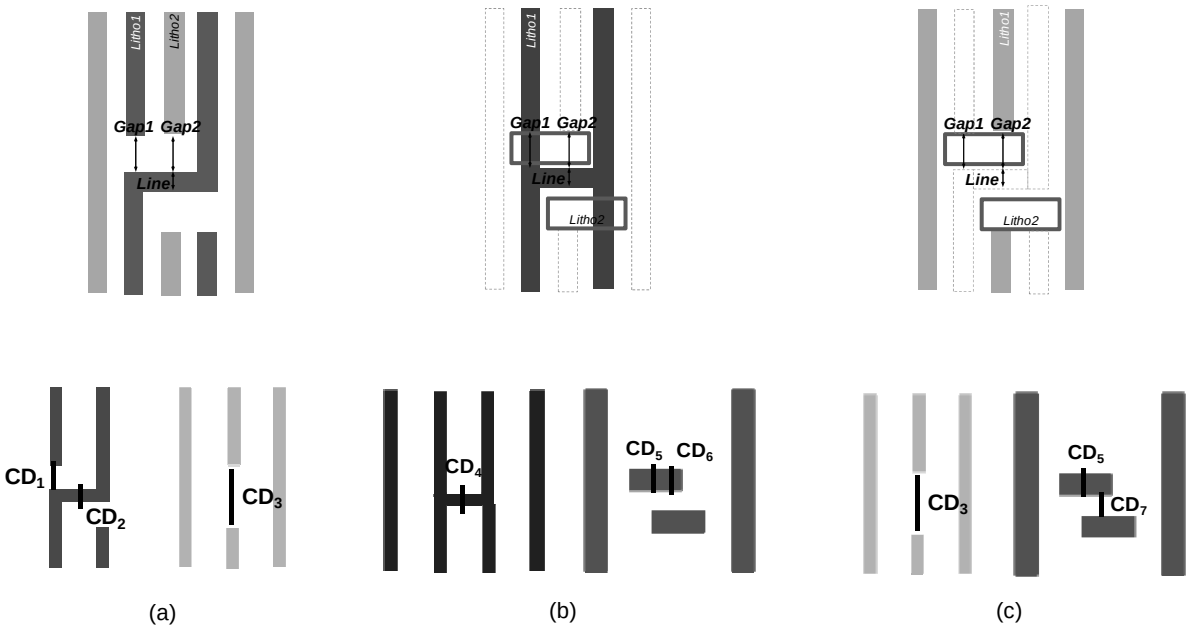


Figure 5 – CD variability definition of both patterning steps for every decomposition style, **a)** LELE scheme, **b)** SIT 1st decomposition (SIT1) and **c)** SIT 2nd decomposition (SIT2)

$$Gap1(3\sigma) = \sqrt{CD_1^{\,2} + Etch_1^{\,2}} \tag{2}$$

$$Gap2(3\sigma) = \sqrt{\left(\frac{CD_2}{2}\right)^2 + \left(\frac{CD_3}{2}\right)^2 + OVL^2 + \left(\frac{Etch_1}{2}\right)^2 + \left(\frac{Etch_2}{2}\right)^2} \tag{3}$$

$$Line(3\sigma) = \sqrt{CD_2^{\,2} + Etch_1^{\,2}} \tag{4}$$

On the Figure 5.b we have reported the first decomposition style for Sidewall Image transfer (SIT1). In that process the spacer deposition does not impact the overall variability of *Gap1*, *Gap2* and *Line*. Indeed, the Gap1 variability is exclusively driven by the second exposure step of the block mask with the CD_5 contribution from lithography and the final Etch (*Etch*) as described in the Equation (5). The Equation (6) describes the variability for *Gap2* where lithography contributions from first step (CD4) and second step (CD6) are taken into account as well as overlay (*OVL*) and etching steps (*Etch*). As it is the case for LELE scheme, we can also notice a double CDU distribution between Gap1 and Gap2 due to the fact that the first distance is impacted by single exposure step whereas second one is impacted by double patterning process. Finally the Line variability is only driven by lithographic (CD_4) and etching (*Etch*) components.

$$Gap1(3\sigma) = \sqrt{CD_5^{\,2} + Etch^{\,2}} \tag{5}$$

$$Gap2(3\sigma) = \sqrt{\left(\frac{CD_4}{2}\right)^2 + OVL^2 + \left(\frac{CD_6}{2}\right)^2 + Etch^2} \tag{6}$$

$$Line\left(3\sigma\right)=\sqrt{CD_4{}^2+Etch^2} \tag{7}$$

The last decomposition (Figure 5.c) represents the Sidewall Image Transfer of the second decomposition style (SIT2) where only the first lithographic step is different regarding SIT1. In that case, although there is a slight change on the first lithographic step we can see that spacer deposition as to be taken into account in the definition of the 2D shape structure as well as the gap with the line end (*Gap2*). This a major concern because we see here that the decomposition style is impacting the overall CDU. Equation (8) describes the CD variability of Gap1 which is exactly the same as equation (5) where dispersion is driven by first patterning step. For Gap2 we have to take into account overlay error (*OVL*) and spacer deposition due to the fact that edge of the 2D shape is derived from the spacer growth (*Spacer*) of the first patterning step (CD_3) as well as the definition of the second exposure (CD_7) and a final etching step (*Etch*). Equation (9) allows to calculate the CDU (3σ) of *Gap2*. As mentioned, the horizontal line of the 2D shape (*Line*) is derived from the spacer growth (Spacer) but it is also driven by the whole gap variation of first lithographic step (CD_3) as well as gap of second exposure (CD7). We have to consider the overlay error (*OVL*) and the etching step (*Etch*) to get the final CDU picture of this line as mentioned in equation (10).

$$Gap1\left(3\sigma\right)=\sqrt{CD_5{}^2+Etch^2} \tag{8}$$

$$Gap2\left(3\sigma\right)=\sqrt{\left(\frac{CD_3}{2}\right)^2+Spacer^2+\left(\frac{CD_7}{2}\right)^2+OVL^2+Etch^2} \tag{9}$$

$$Line\left(3\sigma\right)=\sqrt{CD_3{}^2+\left(2.Spacer\right)^2+CD_7{}^2+OVL^2+Etch^2} \tag{10}$$

These equations will allow us to determine the 3σ CD uniformity of the critical dimension of an Mx jog structure at 64nm pitch. For the calculation we propose to use process data assumption for overlay, etching and spacer deposition steps. Concerning lithographic contributions we do not have measured data so we propose to emulate them based on simulation of the total lithographic budget. We have reported in the table 1 the process assumptions we made for the CDU calculation.

	Etch	***Spacer***	***Overlay***	***Focus***	***Dose***	***Mask***
Dispersion (3σ)	1nm	1.5nm	3nm	25nm	1%	0.5nm

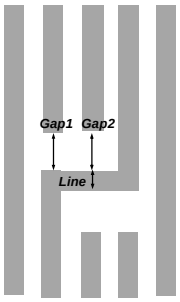
Table 1 – Dispersion values (3σ) used for the CDU calculation of LELE and SIT double patterning scheme

We propose to make a comparison between single exposure process at 90nm pitch with a CD target of 45nm and double patterning process with a pitch of 64nm and a CD target of 32nm. For the simulation we consider an Annular source with partial coherence [0.6/0.8] at 1.35NA and XY polarization for the single patterning process. Concerning the double patterning process, we consider a Quasar source with XY polarization and 30° of pole opening angle for a partial coherence [0.85/0.97] at 1.35NA. The simulations have been performed using Panoramic technology. For the rest of the paper we propose to represent the CDU (3σ) in percentage of the CD target in order to make some cross comparison between single and double patterning scheme.

On Figure 6 we have reported the CDU (3σ) in percentage of CD target, of the Mx jog structure for *Gap1*, *Gap2* and *Line* in the case of single exposure step, LELE, SIT1 and SIT2. In these results we can see that the single

exposure technique has the same variability whatever the dimension is, and it is 9% of CD variability. The *Gap1* dimension for LELE is performed during the first patterning step, this is thus resulting in a similar CDU of 9% regarding single exposure step. In the case of SIT1 and SIT2 we can highlight the fact that the variability is less than single exposure step (5% versus 9%). This is due to the fact that in SIT process the variability of Gap1 is exclusively driven by the second exposure step which is a line of resist to define this dimension. We have a better CD control on a resist line rather than on the gap between two trench-ends, that's for why we obtained a lower variability with the SIT process than LELE or either single exposure.

In the case of *Gap2* and *Line* we see an important degradation of the CDU for LELE and SIT process regarding single exposure step with 1.5x to 2.5x CDU degradation. These degradations are coming from the added process steps involved in the double patterning scheme. In the case of the largest CDU values, 24% for *Line* in LELE and 19% for *Line* in SIT1, it is exclusively due to lithographic process. Effectively, in that case the main contributor to CDU is the CD variation of the first exposure step with 23% for LELE (distance CD_2) and 18% (distance CD_4) for SIT1.



	Gap 1	Gap 2	Line
Single Exposure	9%	9%	9%
LELE	9%	16%	24%
SIT 1	5%	14%	19%
SIT 2	5%	12%	16%

Figure 6 – CD uniformity (3σ) calculation results for Mx 2D shape structure in the case of single exposure, LELE, SIT1 and SIT2 process flow

These structures are "super critical" in the sense that it is necessary to print small line of 32nm width in a semi-dense configuration (pitch 128nm). In the case of SIT2, the lithographic contribution is smaller compared to the others splitting techniques with a variability of the dimension CD_3 of 8% (overall CDU for *Line* SIT2 is 16%). The main lithographic contributor for SIT2 comes from the first exposure step which present a less critical structure than the other technique with the necessity of printing a gap of 152nm (CD_3), a CD width of 32nm with 128nm pitch.

In the case of the "super critical" configurations, there is no room to insert supporting SRAF and the lithographic process is mainly controlled by the source performance. Printing small lines of 32nm in a semi-dense configuration (line/space ratio of 1:3) leads to a process window that is not at the isofocal regarding single exposure step with 1:1 line/space ratio.

If we look at the features after decomposition on Figure 1, it appears that there are four different structures depending on the decomposition style we used. Three structures are quite regular (*Litho1* and *Litho2* of LELE and *Litho1* of SIT process) and one structure looking such as random dots (*Litho2* of SIT process). We propose then to use RET solution to enhance the overall lithographic process window of each of these structures. Source optimization (SO) is well suitable in case of regular pattern due to the fact that the SO process is optimum for periodic structures. In the case of random dots we plan to use model-based SRAF (MB-SRAF) in order to improve the placement of the scattering bars and gain some process window.

4. RET IMPROVEMENT

Brion's Tachyon Source-Mask Optimizer (SMO) is used to co-optimize the scanner source and the mask design simultaneously[5]. Since its beginning it has been integrated with ASML scanners and Brion computational lithography solutions to enhance lithographical performance even further. The optimization flow, which is a true co-optimization of the source and mask based on Edge Placement Error, can be customized by the user depending on the specific applications. In our case, Tachyon SMO has been used to optimize the freeform source

for various sets of structures in both vertical and horizontal orientations. Each set of SMO has been optimized using four cells. The first two are anchor features in horizontal and vertical direction at CD of 32nm and pitch of 128 nm. The last two cells are the "super critical" structures of the splitting techniques in both directions. The SMO flow requires several input parameters for the optimization: input model, cell windows, DOE type and process information. We selected a full resist model as input for Tachyon SMO. This model has been previously calibrated using standard methods for model calibration. Source-only (SO) optimization has been selected and by fixing the mask and adjusting the source to achieve an optimized result. The flow can output various source types. The freeform source which is a pixilated source has been chosen as a source type for the optimization. The optimization based on Edge Placement Error (EPE) minimization is performed through seven evaluation conditions at the +/- 40 nm defocus, +/- 3% delta dose and +/- 0.5 nm mask error offsets.

Figure 7 illustrates the output of the optimized source for the three different structures coming from LELE and first lithographic step of SIT process. We can see that the SO process has made some slight modification of the source shape regarding the initial Quasar shape that has been used for first lithographic simulation. We can see that the optimization process acts essentially for *Litho1* structures of LELE process (Figure 7.a) and *Litho1* of SIT1 process (Figure 7.c). Concerning the *Litho2* of LELE and *Litho1* of SIT2 (Figure 7.b) the SO process changes are minor and the output source is close to the initial Quasar shape.

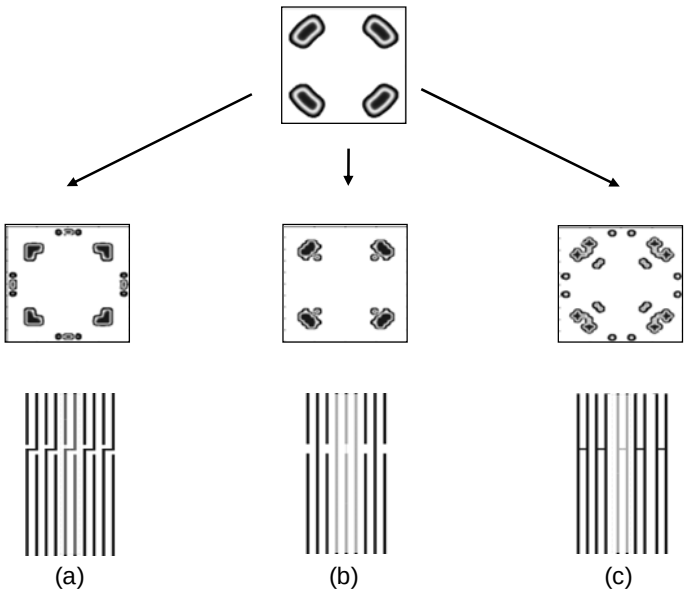


Figure 7 – Source shape outputs after SO process for **a)** *Litho1* of LELE process, **b)** *Litho2* of LELE and *Litho1* of SIT2 process, **c)** *Litho1* of SIT1 process

On Figure 8 we have reported the Bossung curves for the Litho1 structures of the SIT1 process. It represents the CD variations through dose and focus of the CD4 distance with a targeted value of 32 nm at nominal condition. The Bossung with the Quasar illumination is represented on the Figure 8.a and with the SO source on the Figure 8.b. We can see here that the CD variations through the process window have a curvature more important with the Quasar illumination than the optimized SO source. It indicates that the source optimization process allows to move the process toward the isofocal (curvature equal to zero).

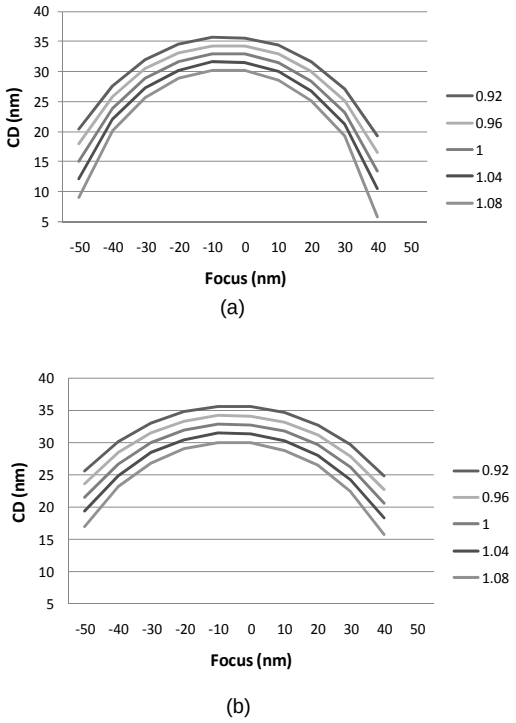


Figure 8 – CD variations through dose and focus (Bossung curves) of the distance CD_3 of the Litho1 of SIT1 process, **a)** for Quasar 30° [0.85 0.97] XY polarization and **b)** for SO source

In the case of *Litho2* for the SIT process presenting random dots we have applied a model-based SRAF solution provided by Brion technology. The principle consists in simulating the intensity map and use it as a guidance map for scattering bars placement. The SRAF candidates are then inserted at places where it enhances the contrast of the main pattern. Then a final cleaning step is applied to reach DRC specifications. On the Figure 9 we have reported the scattering placement with a rule-based method (Figure 9.a) and after model-based method (Figure 9.b). We can see some modification of the SRAF width and position with the model-based versus the rule-based one.

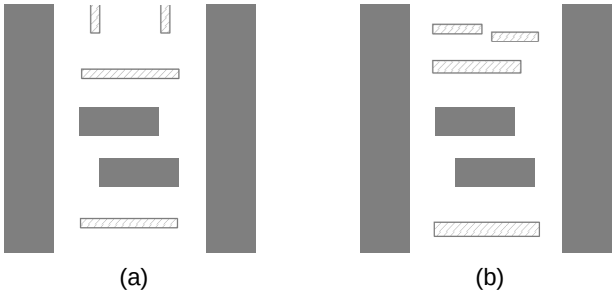


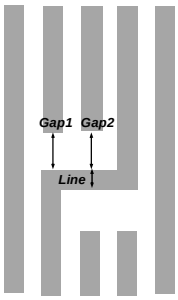
Figure 9 – SRAF placement for Litho2 of SIT process, **a)** Rule based placement, **b)** Model-based placement

In the table 2 we have reported the CD variation (3σ) before and after RET optimization of each dimension from CD_1 to CD_7. Note that CD_1 to CD_4 dimension have been optimized using SO process and CD_5 to CD_7 have been enhanced using MB-SRAF solutions. The most important improvement concerns the "super critical" structures CD_1, CD_2 and CD_4 where the CD variability have been improved from 1.5x to 2x.

	CD_1	CD_2	CD_3	CD_4	CD_5 - CD_7
CDU reference (3σ)	8%	23%	18%	7%	4%
CDU improvement (3σ)	7%	14%	12%	5%	3%

Table 2 – CDU (3σ) for lithographic step before and after RET optimization

We introduce these simulated data improved by the RET optimizations within the overall CDU calculation of the *Gap1*, *Gap2* and *Line* distance of the Mx jog structure. The results are reported on the Figure 10 where we can see a great improvement of the CDU in the case of LELE process and SIT1 process with a 1.5x to 2x CDU enhancement regarding reference process. Concerning the SIT2, RET improvement is quite low with only 1% gain on the overall CDU. It is essentially due to the fact that the CDU of this decomposition style is not driven by lithographic step but have added contributions regarding other splitting techniques such spacer deposition (see equations 8 – 10).



	Gap 1	Gap 2	Line
LELE	8%	12%	14%
SIT 1	4%	12%	12%
SIT 2	4%	11%	15%

Figure 10 – CD uniformity (3σ) calculation results for Mx 2D shape structure in the case of LELE, SIT1 and SIT2 process flow

After RET optimization we see that the SIT1 process offers the best CDU control regarding SIT2 and LELE process. Gap1 distance has a CDU below single patterning step (4% versus 9%) and Gap2 and Line distance have CDU of 12%. In addition to the "computational" tricks, we can also consider hardware optimization to improve the overall CD uniformity such as dose control[6].

5. CONCLUSION

We have presented in this paper a comparison of double patterning techniques for metal-X layers with sub resolution pitch of 64nm. We have made a CDU analysis on 2D shapes jog structures in the case of Litho-Etch-Litho-Etch scheme and Sidewall Image Transfer process. We highlighted the fact that double patterning scheme presents 2 ~ 3x CDU degradation regarding single patterning process. This is due to the increase of process steps where we have to consider multiple lithographic, etching, spacer deposition and overlay contributions. Moreover it appears that in a double patterning scheme we have to print feature in semi dense configuration that leads to lithographic process capability which is not at the isofocal. This limitation in terms of lithographic performance is one of the key constraints on the overall CD uniformity. We have shown that advanced RET solutions such as source optimization and model based SRAF placement allows to overcome this problem by enhancing the lithographic performance and move the CD variation through dose and focus towards the isofocal. We have also shown that the decomposition style is a key factor on the CD process control. Thus this decomposition style has to be taken into account during splitting rules definition. In that sense it is preferable to have the 2D shape (polygon with more than 4 vertices) on the first lithographic step in the case of SIT process. By this way, the spacer deposition is not taken into account in the overall CDU leading to a better control of the process. The sidewall image transfer technique offers the best option in term of CDU control with lower variability on line-

end definition than single exposure step and better CDU control on 2D shapes distance compared to LELE process.

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